**Team NOR Project Report**

Progress:

Team Nor has successfully built 16 bit components of an Adder, Subtraction, Shifter, And gate, Or gate, and Pass A for the ALU. We also created a 16b 8:1 Mux to take in the 16 bit values from our built components and our arbitrary function. This Mux is used in the top-level connections. A 16-bit register was built as well to store the values of A, B, and out.

The And gate, Or gate, Pass A, and a 8:1 Mux were built for design review 1. Adder, Subtraction, Shifter, and Register were built and simulated for design review 2. The 16b register was made out of a master and slave latch. The latches were built from the 2:1 Mux that we previously created from the bonus section in design review 1. The 16b 8:1 Mux was created from the 8:1 Mux we already had.

Currently all inputs feed into the ALU 7 function circuits and then the outputs of each function are fed into a 16 bit 8:1 Mux controlled by the three S control bits. We later will design a decoder to split the inputs into 7 in order to conserve power by not completing each arithmetic function when only one is desired, but for now we are directly feeding the inputs into the inputs of each function. For the no-op the output of the Mux is fed back into its input which crates no change in the output.

The 16-bit Adder was created by using a 16 1b mirror adders. The mirror adders were inverted for every other bit. To make the 16 bit Subtraction we turned the 16 bits from the B input into 2s complement by inverting B and adding 1. Then we took the A input and the new B input and put them into the 16-bit Adder that we made. Currently this is a waste of space, but we plan on fixing this later. We created the 16-bit Shifter by created a 1b Shifter, each with four outputs that had two transmission gates that were fed b1 and b0 (controls). This allowed for each combination to make the input go to the correct output. We then created 16 of these for each input and connected the outputs such that for any combination of b0 and b1 only the correct input was fed to the output, such as to shift the input the amount of bits required.

A useful item that we decided to create is a “master netlist” with all of our subcircuits. All of the subcircuits were commented out. This way when it came time to simulating, all we had to do was on comment the component that we wanted to test. Team Nor came up with a table to measure delays for the Adder, Subtraction, Shifter, And Gate, Or Gate, and Pass A, all of which can be seen in the report. Also, we made a final decision for our arbitrary function; a Multiplier! We discover the best ratio for the PMOS to NMOS is 1.66 rather than 2:1. To do this we connected the inputs to the outputs of an inverter. We iterated through the ratios until we found the value closest to vm = vdd/2.

Remaining Tasks:

We need for create a multiplier and simulate it. Also, we need to build a decoder for the ALU. As we previously said, the subtraction component has to be made smaller. Another task is to finish connecting all of the pieces. Team Nor still needs to improve our delay, by implementing the 1.66 ration of PMOS/NMOS that we discovered. Our last assignment is to create a final presentation.